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Research Article

Design of High Gain Single Stage Telescopic Cmos Operational Amplifier

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Abstract

A need for high gain operational amplifiers (op-amps) exists for certain applications. This requires research in the area of its gain without affecting other parameters drastically. In this paper, high gain single stage Telescopic CMOS operational amplifier has been designed and verified, using PSPICE simulation software. The designed circuit operates at ±5V power supply in the 1 µm CMOS technology. The simulation results show that the proposed single stage Telescopic CMOS op-amp has an open loop gain of 77.777dB, unity gain frequency of 7.3054MHz, ICMR of -0.248V to 4.4120V and output voltage swing of 7688.8 times to that of input. A 2pF load capacitor is applied in performing a stable phase margin of 80.669 °. As result shows that the designed circuit has high gain, which is used for various applications where very large gain is required to amplify weak signals, such as heart beat in medical instrumentations. The total power consumed by the device is 0.589mW. This shows that the power consumed by the device is too small. Therefore, this device can operate for longer duration of time. The smaller the power dissipation the better the device is. Low power operation is a very important quality factor for batteries that should supply the system for hours or days to power more and more electronic systems.

Keywords

Weak Signals, Single Stage CMOS Op-Amp, PSPICE Software

1. Introduction

1.1. Operational Amplifiers (op amp)

The name of operational amplifier found its name due to its performance in mathematical operations (addition, subtraction, integration and differentiation) [1, 2]. It is a five-terminal device as shown in the figure 1 below [3].

Op-amp is very large gain material which amplifies the difference of its two input voltages [4]. If input is applied to the non-inverting terminal, we will get amplified output with the same polarity with input [6]. Whereas if we apply the input to the inverting terminal will get amplified but inverted output [5-7]. Op-amps are electronic devices which are mostly today [8]. Such as: used in a wide array of consumer, industrial, medical and scientific devices, etc. [8].

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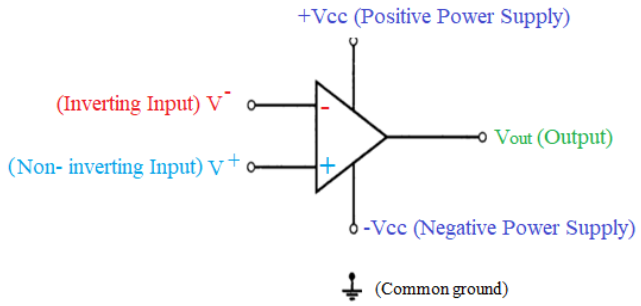

Figure 1. *Symbol of Op-amp [3].*

1.2. Performance Parameters of op-amp

To designing op-amp we must consider many important performance parameters, which indicate quality of op-amp [5]. The following are the main performance parameters that indicate the efficiency of op-amp.

Open loop Voltage gain (A_O): it is obtained by taking the ratio of the output voltage (V_O) to differential input voltage (V_d) within open loop circuit [5]. The open loop gain of an operational amplifier is not varying at very small frequency; however it decreases very fast with exceeding frequency see figure 2 [9].

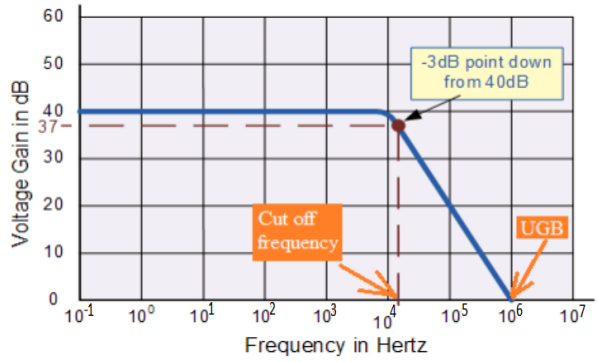

Figure 2. *Gain verses frequency of practical op amps [6].*

The unity-gain frequency (UGB): Is the value of frequency at where gain reduces to zero dB or unity [10].

Common Mode Rejection Ratio (CMRR): It is obtained by taking the ratio of magnitude of differential voltage gain to the common mode gain [7]. It shows that strength of an op-amp to reject noise, and magnifies any signals that are differential between them [7].

Input common mode range: It is the very large range of the common-mode input voltage which does not generate a significant difference on differential gain [3].

Phase margin (PM): It indicates the phase shift of the amplifier at the unit gain bandwidth [8]. Therefore, it measures the stability of op amp [1, 8].

Output voltage swing: It is the maximum output voltage that the op-amp can produce before clipping for certain load and working applied voltage [11].

Slew Rate (SR): Is the ratio of output voltage for a step-signal input to time [7]. Therefore, in other words it is the measure of the slope of the output voltage (V_{Out}) [7].

Mathematically it is given by:

$$SR = \left(\frac{dV_{Out}}{dt}\right)max \quad (1)$$

Unit of slew rate is V/μs [8]. For ideal op-amp slew rate is infinity [7]. The output reaches at the same instant of input application [7]. This shows that the input reaches to the output without losing of time [9]. We can get largest slew rates in op-amps by using high frequencies [9].

Total power dissipation (PD): Is the power used by the device [8]. Ideally op amp does not use any power. However practical op amp dissipates finite power [9]. If the power used by the device is low, then it can operate for long time [7-9]. The lower the power dissipation the better the device is [9].

1.3. Types of CMOS Operational Amplifier Topologies

We can classify op-amp topologies in to four. These are single stage op-amp, two stage op-amp, Folded- cascode op-amp, and Telescopic op-amp [12-16].

Single stage CMOS operational amplifier

Single stage CMOS op-amp has small size to design as shown in the figure 3 [12]. It has small gain due to its small output impedance [14-30]. But, its small output impudence leads to large unity gain bandwidth and large speed. Due to large speed it has small power dissipation [12-16].

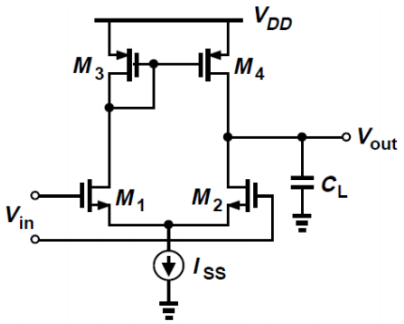

Figure 3. *Single stage CMOS op-amp [16].*

Single stage Telescopic cascode CMOS op-amp

Figure 4. shows topology of telescopic cascade op-amp. In order to obtain larger gain than single stage, we can use cascading (transistors are cascaded between the power supplies in series) [15, 16]. Single stage op-amp has smaller gain than telescopic cascade op-amp [16-18]. Disadvantage of this topology is the very small output swing. Due to its high speed telescopic op-amp has low power dissipation [15-20].

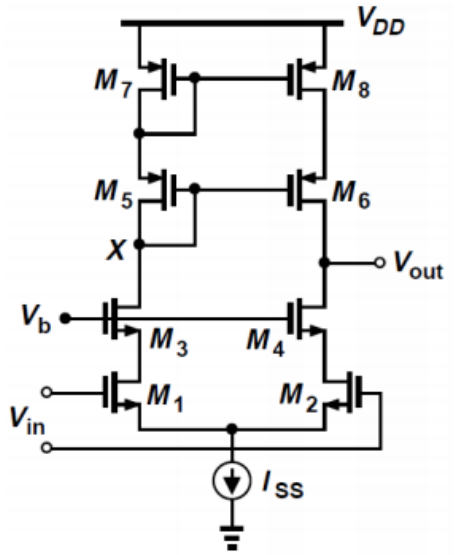

***Figure 4.**. Single stage telescopic cascode op-amp [17].*

Folded cascode op-amp

In order to solve some of the disadvantages of telescopic op-amps such as limited output swing, we can use a "folded cascode" as shown figure 5 [21-23]. This topology lies between telescopic and two stage op-amps. It has low supply input voltage [22]. However due to its high output impendence, high power dissipation and low speed folded cascode op amp has larger output voltage swing [24]. The gain of the folded cascade is smaller than the two stage op amp, but greater than telescopic [22-24]. Telescopic cascade op amp has larger speed folded cascode op amp [21-24].

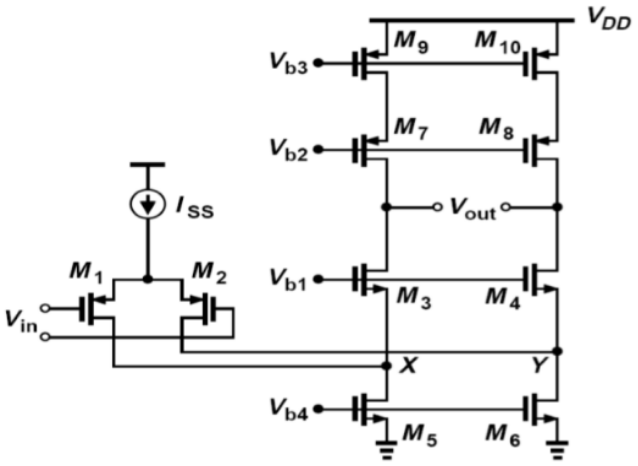

***Figure 5.** Folded cascade op-amp [25].*

Two stage op-amp:

In order to design amplifiers with both large gain and high swing, one must apply two-stage amplifier as shown in the figure 6 [26-28]. First stage of two stage op amp is used to produce high gain, whereas second stage produces large swing [27-29]. But, it has compromised frequency response, large power consumption (because of two stages), and small speed and has very low power supply rejection at high frequencies [26-30]. The larger output swing produced by the second stage is used for some applications, mostly with lower supply voltages in today's technologies [10, 17].

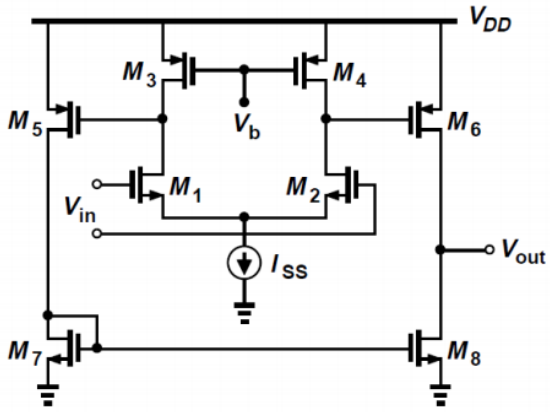

***Figure 6.** Two-stage op-amp [17].*

2. Methodology and DESIGN Techniques

2.1. Schematic Layout

Usually there are many topologies used for a particular functionality. The designer has to choose an appropriate circuit topology which meets the specification. The topology of the circuit to be designed in this research work is a single stage telescopic CMOS op-amp, shown in figure 7.

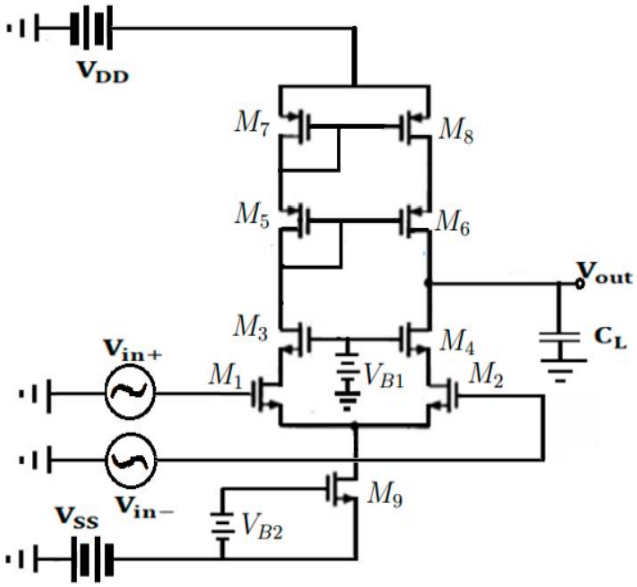

***Figure 7.** Single stage Telescopic CMOS op-amp lay out [10].*

The circuit consists of nine transistors: out of which five (M_1, M_2, M_3, M_4 and M_9) are NMOS and the remaining four M_5, M_6, M_7 and M_8 are PMOS transistors. Transistors M_1 and M_2 form the basic differential input stage. Since NMOS transistors give more current source and gain than PMOS transistors [3]. That is why we choice NMOS transistors in differential input rather than PMOS transistors. The gate of M_2 is the inverting input and the gate of M_1 is the non-inverting input. The differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage, which is simply the Trans-conductance of M_1 times the total output resistance seen at the output.

The transistors M_3 and M_4 are used to convert differential input signal in to single output signal. While the transistors M_5, M_6, M_7 and M_8 used to increase the output swing and the gain. The transistor M9 act as current source and it is expected to give more drain source current.

The gates of M_9 should be biased by a voltage that keeps it in saturation. The gates of M_3 and M_4 should be biased by a voltage that keeps both M_1 and M_2 in saturation and which, at the same time, should avoid M_3 going into triode region.

2.2. Design Specifications

Generally, the idea behind any design procedure is to get a circuit that meets certain specifications. Therefore, the single stage telescopic CMOS op-amp designed in this study is expected to meet the specifications listed in table 1. The design of a single stage telescopic CMOS op-amp uses 1 µm CMOS technology.

Table 1. *List of specifications for single stage Telescopic CMOS op-amp.*

Parameter	Proposed value
Open loop gain	≥40dB
Load capacitance	2pf
UGB	≥1MHz
ICMR	1.12V to 1.4V
Supply Voltages (V_{DD}, V_{SS})	(5V, 5V)
Power dissipation	≤10mw
Phase margin	≥45°

Table 2. *List of constant parameters and boundary conditions.*

Constant parameter	Value
Tail current	≤99µA
Constant parameter for NMOS (K_n)	99.7 $\frac{\mu A}{V^2}$
Constant parameter for PMOS (K_p)	24.1 $\frac{\mu A}{V^2}$
Thresh hold voltage for NMOS ($V_{th,n}$)	0.65V
Thresh hold voltage for PMOS ($V_{th,p}$)	-0.65V
Minimum length (L)	1µm

2.3. Design Procedure

All the transistors in the design are expected to be in saturation mode of operation. Since to use transistor as amplifier, they must be in saturation region unless output signals become distorted and nonlinear [8]. The procedure and basic relationship that we have used in the design process are described as follows:

Step 1: we must estimate the tail current (I_T), by using definition of slew rate. i.e.:

$$I_T = SRxc_L \tag{2}$$

Step 2: Design tail transistor M_9 by calculating its width (W) and length (L) by using the transistor in saturation equation. The equation used is:

$$(\frac{W}{L})_9 = \frac{2I_T}{K_n(V_{GS9}-V_{th,n})^2} \tag{3}$$

In addition bias voltage V_{B2} of transistor M_9 is equal to its gate source voltage. i.e

$$V_{B2} = V_{GS9}$$

Step 3: Design the differential pair of the circuit (M_1 and M_2) by assuming both of them to be working in saturation mode, and the current moving through them is half of the tail current. Their aspect ratios could be calculated using the following equation.

$$(\frac{W}{L})_{1,2} = \frac{I_T}{K_n(V_{GS1}-V_{th,n})^2} \tag{4}$$

Step 4: Design transistor (M_3 and M_4) by assuming the two transistors used are identical and in saturation mode. Calculate their aspect ratios by using the following equation.

$$(\frac{W}{L})_{3,4} = \frac{I_T}{K_n(V_{GS3}-V_{th,n})^2} \tag{5}$$

Where:

$$V_{GS3} = V_{B1} - V_{ds,sat9} - V_{ds,sat1}$$

By assuming bias voltage, $V_{B1} = 0.64V$

Step 5: Design the Cascode Current Mirror stage (M_5, M_6, M_7 and M_8) where there are four PMOS transistors by assuming the drain source current passing through them is similar to the drain and gate are tied to each other. The transistors M_5, M_6, M_7 and M_8 will be designed by using equation 2.5 and 2.6 respectively.

$$(\frac{W}{L})_{5,6} = \frac{I_T}{K_p(V_{GS5}-V_{th,p})^2} \quad (6)$$

Where $V_{GS5} = V_{DD} - 3V_{th,p}$

$$(\frac{W}{L})_{7,8} = \frac{I_T}{K_p(V_{GS7}-V_{th,p})^2} \quad (7)$$

Where, $V_{SS} + 3V_{th,n} + V_{GS7} + V_{DD} = 0$

2.4. Mathematical Formulations

We can estimate the tail current by using equation (2) as follow as:

$$I_T = SRxc_L = 1\frac{V}{\mu s}x2pF = 2\mu A$$

From boundary condition $I_T \leq 99$ µA. by taking large current ensures all transistors to operate in saturation region. So, take tail current as 58.92 µA.

Tail transistor M_9may be designed by using the equation 3. i.e.

$$(\frac{W}{L})_9 = \frac{2I_T}{K_n(V_{GS9}-V_{th,n})^2} = \frac{2*58.92A}{99.7\frac{\mu A}{V^2}(0.16V)^2}$$

Since we assume that input pair $V_{GS9} - V_{th,n} = 0.16V$

$$(\frac{W}{L})_9 = 46.21$$

We are taking L as 10 times the technology parameter. Thus, W and L of transistor M9 are:

$$W = 462.1\mu m$$

$$L = 10\mu m$$

We assume that VB2=0.8V

The differential pair of the circuit (M_1 and M_2) may be designed by assuming both of them to be working in saturation mode, and the current flowing through them is half of the tail current. Their aspect ratios could be calculated applying equation (4) as follow as:

$$(\frac{W}{L})_{1,2} = \frac{I_T}{K_n(V_{GS1}-V_{th,n})^2} = \frac{58.92A}{99.7\frac{\mu A}{V^2}(0.16V)^2}$$

$$(\frac{W}{L})_{1,2} = 23.1$$

We are taking L as 10 times the technology parameter. Thus, W and L of transistors (M_1 and M_2) are:

$$W = 231\mu m$$

$$L = 10\mu m$$

Design transistor (M_3 and M_4) by calculating their aspect ratios, by using equation (5). The two transistors used are assumed to be identical and in saturation.

$$(\frac{W}{L})_{3,4} = \frac{I_T}{K_n(V_{GS3}-V_{th,n})^2} = \frac{58.92A}{99.7\frac{\mu A}{V^2}(0.32V-0.65V)^2} = 5.4$$

We are taking L as 10 times the technology parameter. Thus, W and L of transistors (M_3 and M_4) are:

$$W = 54\mu m$$

$$L = 10\mu m$$

Design the cascode current Mirror stage M_5, M_6, M_7 and $M_8$where there are four PMOS transistors by assuming the current passing through them is same as the drain and gate are tied to each other. The transistors M_5, M_6, M_7 and M_8 will be designed by applying equation (6) and (7) respectively as follow as.

$$(\frac{W}{L})_{5,6} = \frac{I_T}{K_p(V_{GS5}-V_{th,p})^2} = \frac{58.92A}{24.1\frac{\mu A}{V^2}(3.5V-0.65V)^2} = 1$$

$$(\frac{W}{L})_{7,8} = \frac{I_T}{K_p(V_{GS7}-V_{th,p})^2} = \frac{58.92A}{24.1\frac{\mu A}{V^2}(0.16V-0.65V)^2} = 6$$

We are taking L as 10 times the technology parameter. Thus,

$$(\frac{W}{L})_{5,6}` = \frac{10\mu m}{10\mu m}$$

$$(\frac{W}{L})_{7,8} = \frac{60\mu m}{10\mu m}$$

3. Design, Simulation, and Analysis

3.1. Circuit Design

The single stage Telescopic CMOS operational amplifier has been designed using the proposed schematic layout given in Figure 7 and the aspect ratios calculated. We have used a double supply voltage of $\pm 5V$. The inverting and non-inverting terminals of the circuit were connected to ground. The width and length of the transistors were initially set according to the calculated values in table 2. But the

specifications of current were not meet. Thus, widths of the transistors of device were adjusted through inspection method by repeating the procedure over and over until the desired optimal results were obtained. Redesign was done to meet biasing current and power dissipation specifications by adjusting the widths of the transistors. The modified design with values appearing best for the proposed work is shown in Figure 8.

3.2. Simulation and Analysis

Node Voltage

Ideally, when both inputs of op-amp are grounded (zero volt), the output offset voltage is zero. But practically this is not true. For op-amp designer one main chiriteria is to check the output offset voltage is zero or nearly zero when both inputs are zero. If it is not zero he or she must make the output offset voltage zero or cloth to zero by using input offset voltage. In this design the output offset voltage is not zero, when both inputs were grounded (0V) before using input offset voltage (VIO). But by iterative trial and error method, we were able to reduce the output offset voltage by applying an input offset voltage of 241.68983573μV. The node voltages and the output offset voltage obtained from the PSPICE simulations are shown in the Figure 9. From the figure we observe that the output offset voltage is an extremely low value which is equal to $38.22pV = 38.22X10^{-12}$ (which is almost zero) when both inputs are grounded.

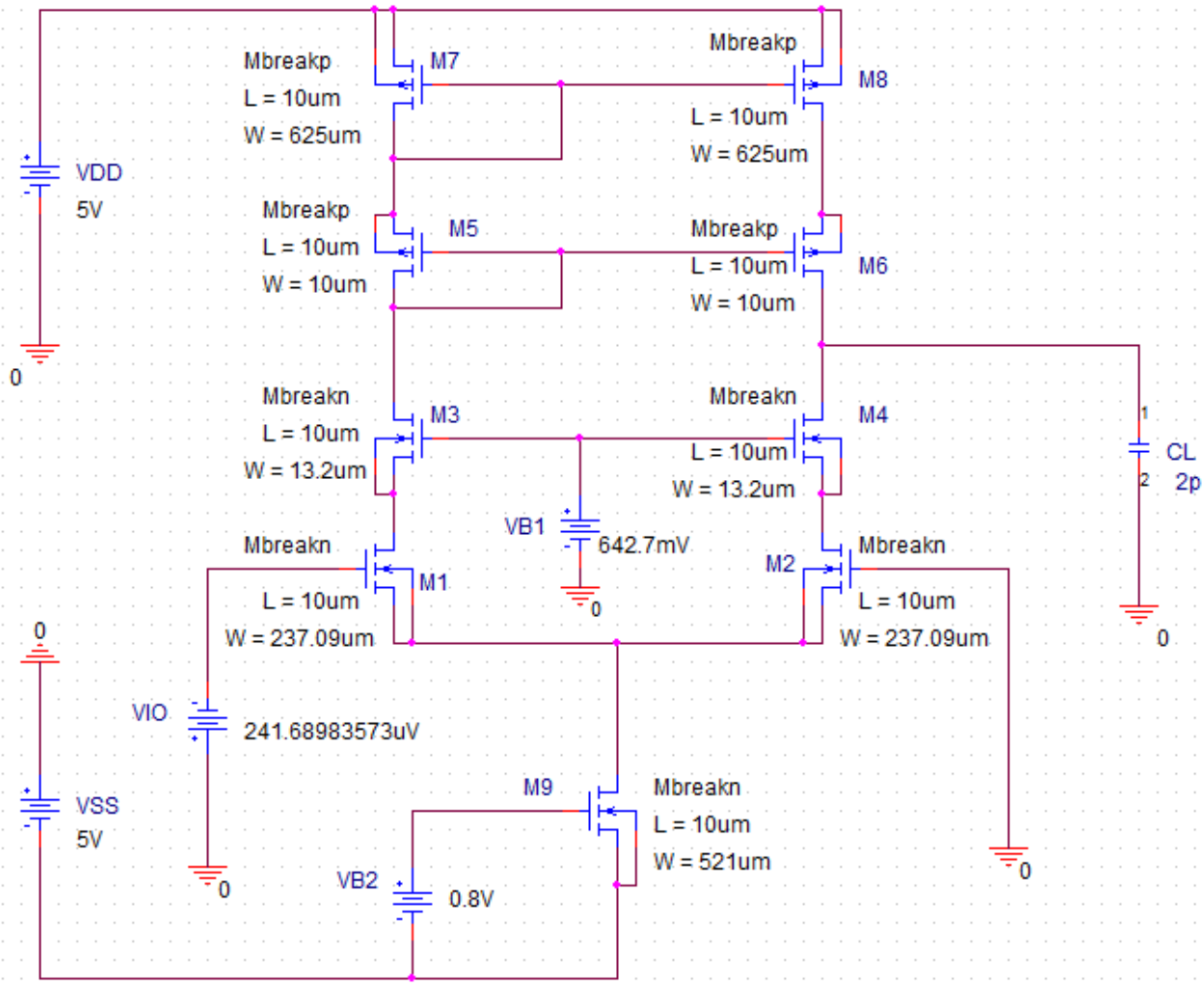

Figure 8. *Single-stage Telescopic CMOS op-amp circuit design.*

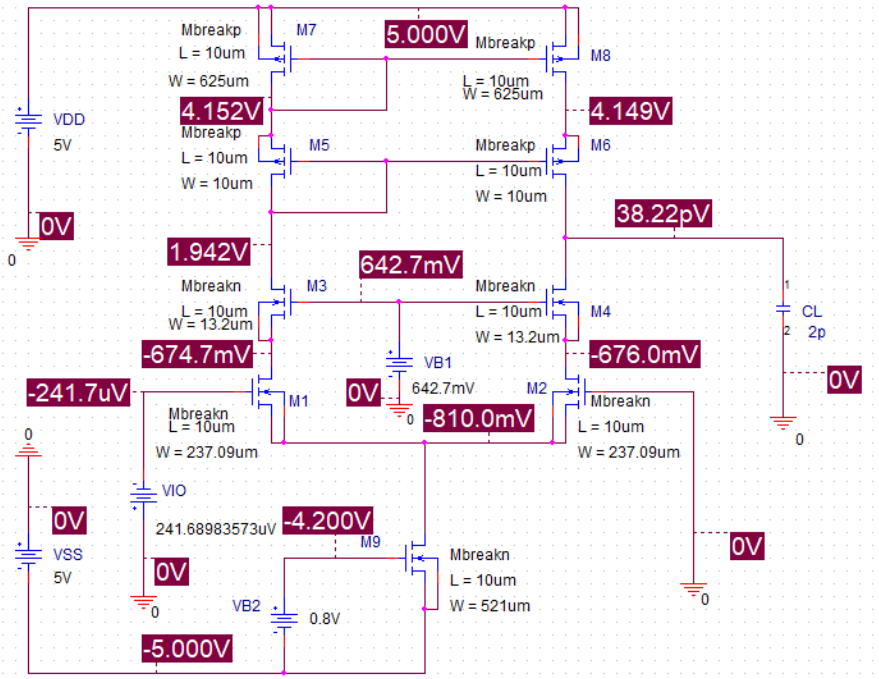

Figure 9. *Simulation results of output offset voltage and node voltages.*

Power Dissipation

Figure 10 shows the simulation results of the power dissipation across each MOS transistor of the single stage Telescopic CMOS op-amp. The total power dissipation (PD) of the circuit is the sum of power dissipation of each transistor. That is:

$$\mathrm{PD} = (3.986 + 3.948 + 77.10 + 19.92 + 65.12 + 122.2 + 24.97 + 25.06 + 246.9)\mu\mathrm{W}$$

$$\mathrm{PD} = 0.589\mathrm{mW}$$

Thus, the total power consumed by the device is 0.589mW. This shows that the power consumed by the device is too small. Therefore, this device can operate for longer duration of time. The smaller the power dissipation the better the device is. Low power operation is a very important quality factor for batteries that should supply the system for hours or days to power more and more electronic systems.

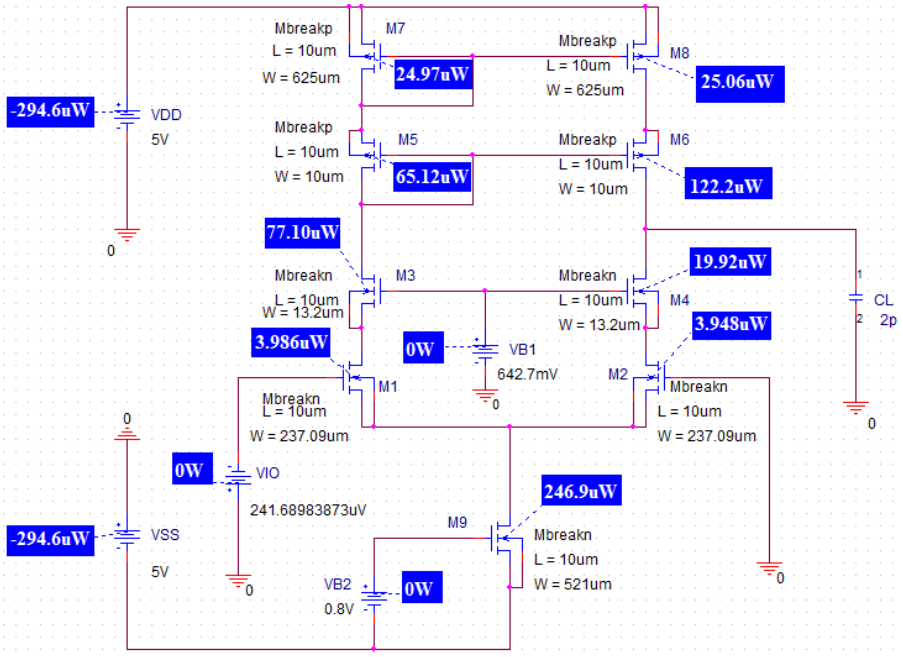

Figure 10. *Simulation result of power dissipation.*

Input Common Mode Range (ICMR)

The circuit design of input common mode range is shown in the figure 11. For linearity test, the single stage Telescopic CMOS op amp is biased in the unity gain (voltage follower) configuration.

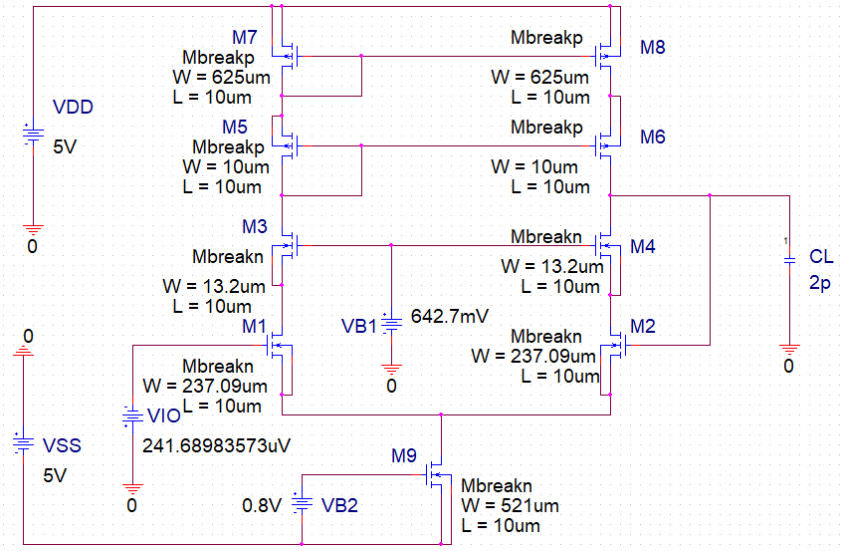

Figure 11. *Circuit design to measure ICMR.*

The simulation result of ICMR is shown in the figure 12. From the figure we can observe that the output voltage of the op-amp is linear for input voltages ranging from -248mV to 4.4120V, for which the output match's with input in magnitude, but it is inverted due to the input offset voltage applied in the non-inverting terminal is negative. Thus, in this voltage range this op-amp is used as a buffer.

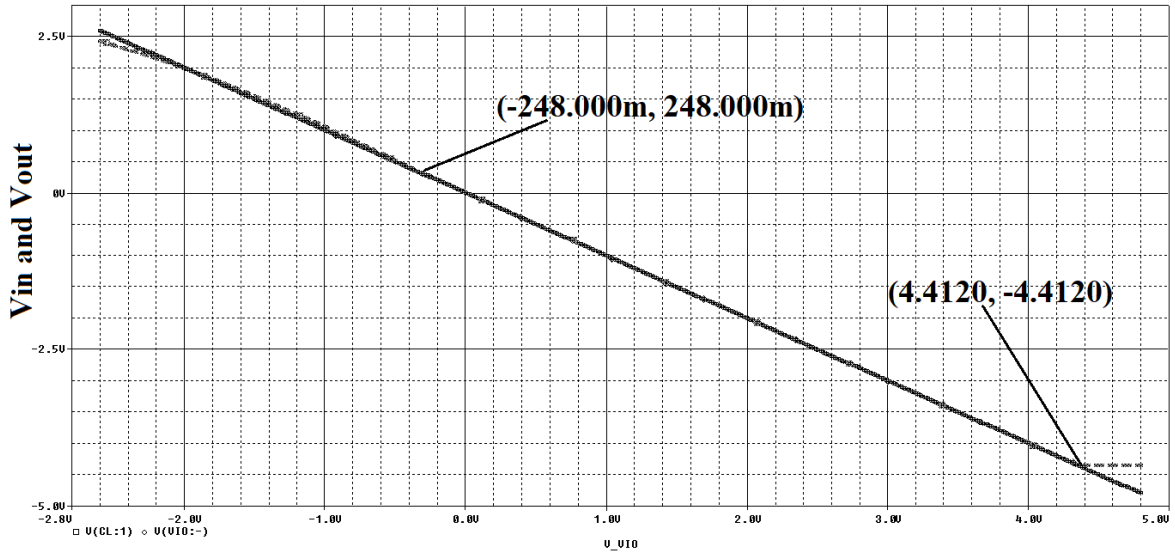

Figure 12. *Simulation result of ICMR.*

Open Loop Gain, Unity Gain Frequency and Phase Margin:

The open loop gain, unity gain frequency (UGB) and phase margin (PM) are measured using the design shown in figure 13. In this configuration the amplifier is an open loop with ±5V supply voltages. An AC signal of 1V is applied at the inverting input terminal and an input offset voltage of 241.68983573 µV is applied to the non-inverting input terminal.

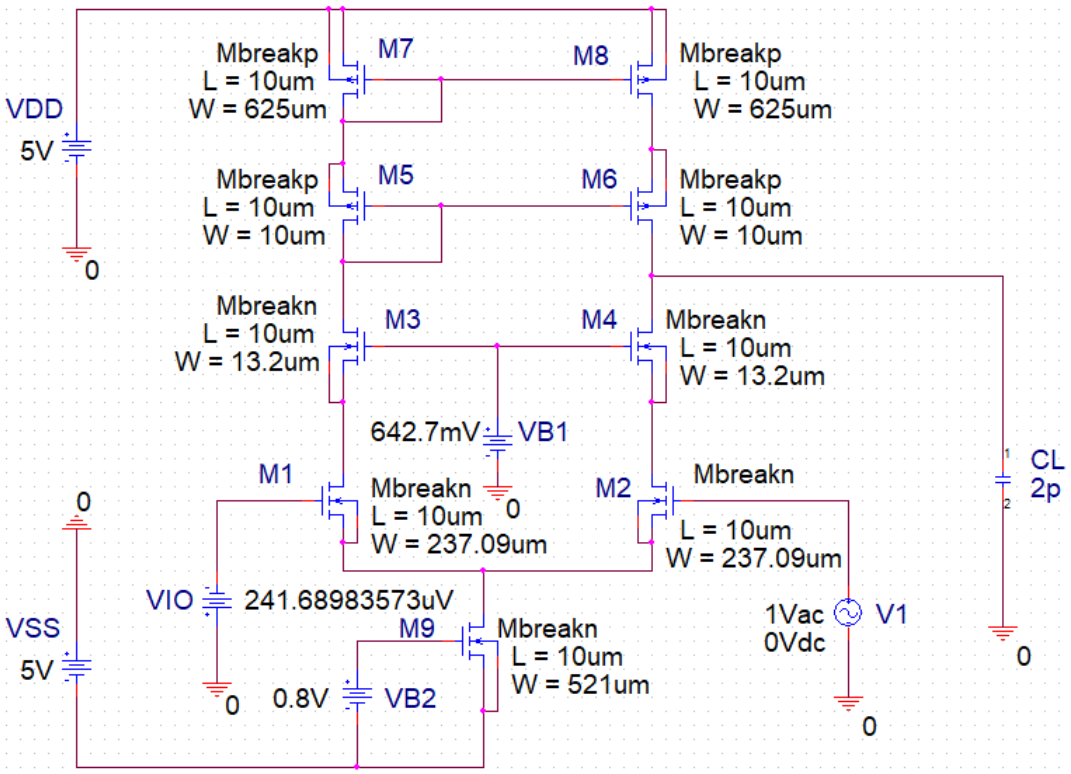

Figure 13. *Circuit design to measure the open loop gain, unity gain frequency, cut off frequency, phase difference and phase margin.*

The simulation results of the open loop gain and the phase margin are shown in figure 14. From the figure one can see that the open loop gain is found to be 77.777dB. Besides the cut-off frequency (the 3dB open loop gain frequency) and the unity gain frequency are 1.9598KHz and 7.3053MHz respectively. In addition, we got a phase difference of 179.971 ºand phase margin of 80.669 º.

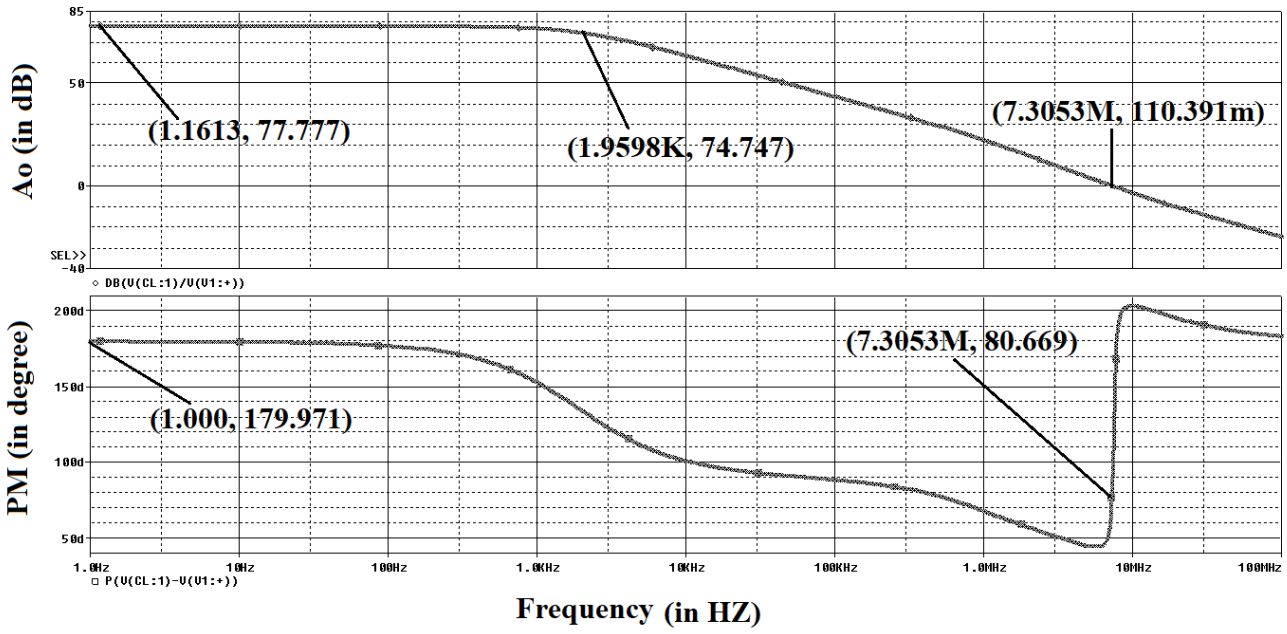

Figure 14. *Simulation result of open loop gain and PM.*

Input and Output Voltage swings:

The circuit design to measure the input and output voltage swings is shown in the figure 15. The inverting terminal is connected to a sinusoidal voltage source of 750nV amplitude with frequency of 100Hz.

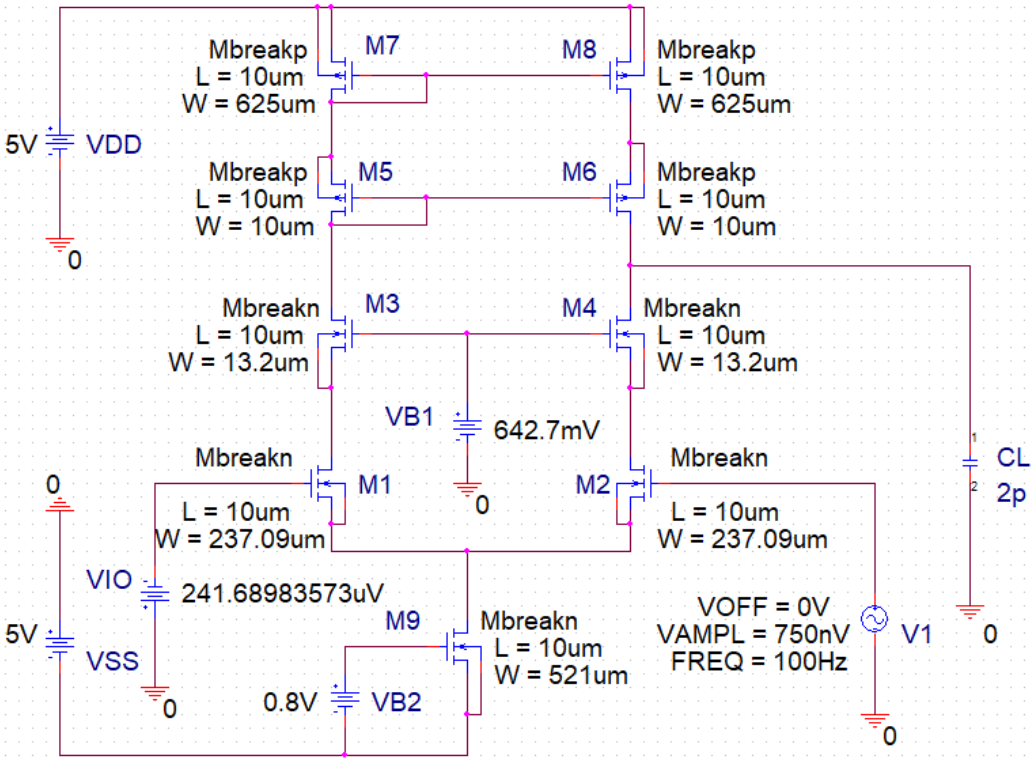

Figure 15. *The circuit design to measure input and output voltage swings.*

The input and output voltage swing simulation results are displayed in the figure 16. As we can see from the figure that output AC voltage is amplified but the input AC voltage lags it by π/2; it is because the input is supplied into the inverting terminal of the op-amp. Also, the peak to peak output signal is 11.533mV**,** when the input peak to peak signal is 1.499976uV.

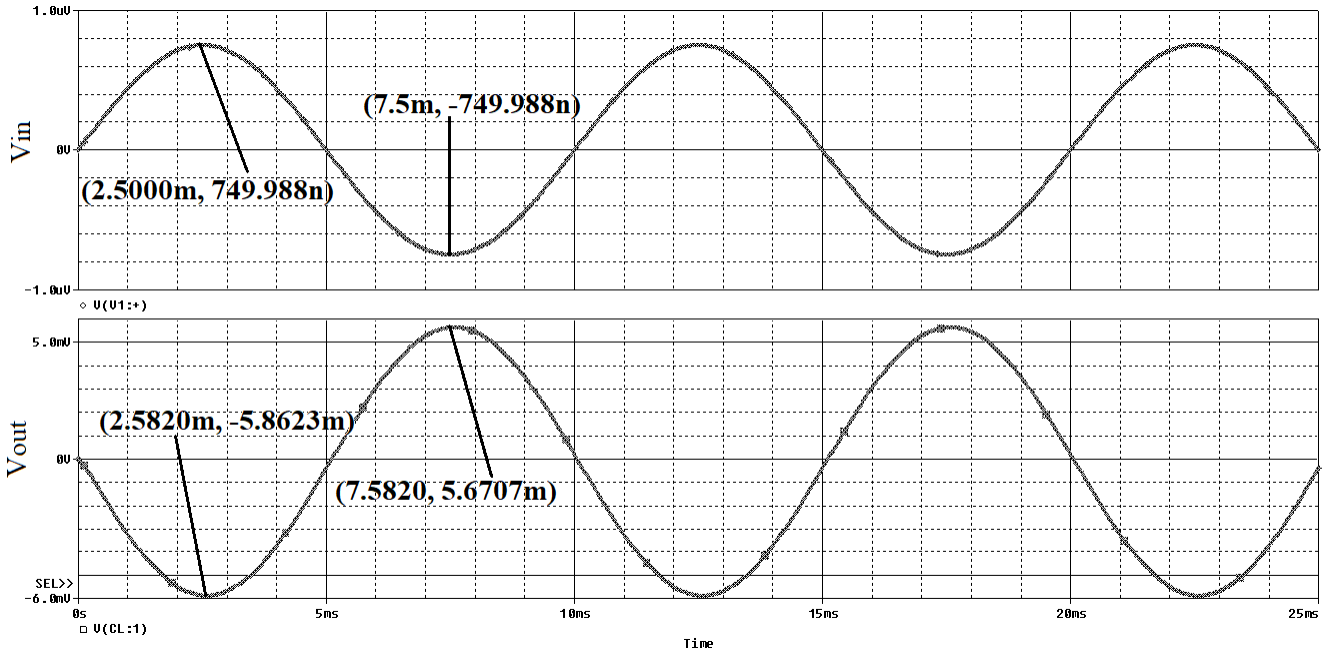

Figure 16. *Simulation result of the input and output voltage swings.*

The gain can be calculated by using gain equation as follows:

$$\text{Gain} = \frac{V_{\text{out p-p}}}{V_{\text{in p-p}}}$$

Where: $V_{\text{out p-p}}$ and $V_{\text{in p-p}}$ are the peak to peak output voltage and the peak to peak input voltages respectively.

Using the values in the gain equation, we get:

$$\text{Gain} = \frac{11.533\text{mV}}{1.499976\text{uV.}} = 7688.78968730166$$

In dB scale the gain can be:

$$\text{Gain(dB)} = 20\log(7688.78968730166) = 77.717\text{dB}$$

Therefore, the output voltage is 7688.78968730166 times the input voltage. The calculated gain is the same as that we have obtained from the graph.

4. Conclusion

In this thesis work, the proposed a single stage telescopic CMOS op-amp has been designed and verified by using PSPICE design and simulation software. By comparing the specification values with that of computer assisted simulation results of performance parameters, we can conclude that a single stage telescopic CMOS op-amp has high gain, large output voltage swing and low power dissipation. Thus, this circuit could be used for various applications where very large gain is required to amplify weak signals, such as heart beat in medical instrumentations.

Abbreviations

op-amp: Operational Amplifier
PD: Power Dissipation
AC: Alternating Current
PMOS: Positive Channel MOS
CMOS: Complementary Metal Oxide Semiconductor
SR: Slew Rate
CMRR: Common Mode Rejection Ratio
V_B: Bias Voltage
DC: Direct Current
UGB: Unity Gain Frequency
dB: Decibel
V_{DD}: Drain Voltage
IC: Integrated Circuit
V_{DS}: Voltage from Drain to Source
ICMR: Input Common Mode Range
$V_{ds,sat}$: Drain to Source Saturation Voltage
C_L Load Capacitance
V_{GS}: Voltage from Gate to Source
A_O Open-Loop Voltage Gain
V_{in}: Input Voltage
NMOS: Negative Channel MOS
V_{out}: Output Voltage
V_{ss}: Source Voltage
VIO Input Offset Voltage
$V_{th,p}$: Thresh Hold Voltage for PMOS
K_n: Constant Parameter for NMOS
$V_{th,n}$: Thresh Hold voltage for NMOS
K_p: Constant parameter for PMOS
L: Length
W: Width
$\frac{W}{L}$: Aspect Ratio
PM: Phase Margin

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Author Contributions

Tsegaye Menberu is the sole author. The author read and approved the final manuscript.

Conflicts of Interest

The author declares no conflicts of interest.

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